L Number	Hits	Search Text	DB	Time stamp
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-	1		USPAT	2004/01/02 12:18
-	1		USPAT	2004/01/02 12:19
-	1		USPAT	2004/01/02 12:19
-	50547	crystal$1 same particle$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:10
-	78	lump$1 and blob$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:41
-	6	(lump$1 and blob$1) and (crystal$1 same particle$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:44
-	1761	microcrystalline near5 film$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:06
-	125	(crystal$1 same particle$1) and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:45
-	598	257/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:52
-	125	(crystal$1 same particle$1) and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:46
-	10	geometr$6 and ((crystal$1 same particle$1) and (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:10
-	3	361/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:54
-	130	428/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:58
-	22	(428/$.ccls. and (microcrystalline near5 film$1)) and (crystal$1 same particle$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:55

-	390	438/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:58
-	1	geometr$6 and ((crystal$1 same particle$1) and (438/$.ccls. and (microcrystalline near5 film$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:58
-	27	(crystal$1 same particle$1) and (438/$.ccls. and (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:59
-	1	solderless same (crystal$1 same particle$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:08
-	1	solderless same (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:08
-	1	connector$1 same (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:09
-	317	crystal$1 same (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:10
-	0	geometr$6 same (crystal$1 same (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:11
-	12	shape$1 same (crystal$1 same (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:11
-	5	wire adj wad$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:40
-	573	wire with button with contact	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:22
-	0	257/$.ccls. and 438/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:50
-	12	257/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:45
-	0	438/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:50

US-PAT-NO: 6563696

DOCUMENT-IDENTIFIER: US 6563696 B1

TITLE: Solderless laser assembly

DATE-ISSUED: May 13, 2003

date not found

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Harris; David B.	Columbia	MD	N/A	N/A
Jablonski; Edward J.	Cockeysville	MD	N/A	N/A
Walter; Thomas A.	Ellicott City	MD	N/A	N/A
Anderson, Jr.; Richard L.	Eldersburg	MD	N/A	N/A

US-CL-CURRENT: 361/619, 165/185 , 165/80.3 , 174/16.3 , 257/675 , 257/706 , 257/718 , 361/704 , 361/707 , 361/760

ABSTRACT:

A connect and disconnect assembly for connecting and disconnecting a laser diode having leads to a printed circuit board (PCB). The assembly includes a heatsink that connects with the printed circuit board by providing cap screws through the PCB which are threadably received in spacers connected to the heatsink. A connection assembly made up of a retainer block and screws connects the laser diode to the heatsink. The laser diode is provided through a cutout portion of the PCB, and connects to the heatsink by providing the screws through the retainer block and the laser diode, the screws being threadably received in the heatsink. A pair of fuzz button carriers are interposed between the laser diode and the PCB. Each fuzz button carrier has a body portion, spaced guide portions extending above the body portion, and fuzz buttons extending through the body portion. When the laser diode is connected to the heatsink, the laser diode leads are provided between the guide portions of the fuzz button carriers and contact the fuzz buttons. The fuzz buttons, in turn, electrically connect the laser diode leads to the PCB pads. The assembly provides a convenient mechanism for connecting/disconnecting the laser diode and heatsink to/from the PCB. Further, the laser diode and assembly can be easily disconnected from the PCB so that a modified, repaired, and/or updated laser diode or other component can be quickly and easily inserted into the circuit without damaging or destroying the laser diode or the PCB.

14 Claims, 5 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Detailed Description Text - DETX (8):

Each fuzz button 46 is a small electrical contact element manufactured from a single strand of fine randomly-woven wire, typically gold-plated Molybdenum (Mo) or Beryllium copper wire, which is die compressed into a cylindrical form. Each strand of wire is typically 0.02 inches in diameter and 0.40 inches in length, although the diameter and length may vary. The random weave of the wire provides multiple connection points at the laser lead 14 and PCB pad 102

interfaces. The resulting object is a solderless wire mass that exhibits excellent spring characteristics and electrical performance. Such contacts are also known as compressible contacts, or compression-based, z-axis connectors. Fuzz buttons 46 are commercially available from Cinch Connector, Inc. of Lombard, Ill. under the trade name CIN:APSE.RTM., and from Tecknit.RTM. USA of 129 Dermody Street, Cranford, N.J. 07016.

Current US Cross Reference Classification - CCXR (4):
257/675

Current US Cross Reference Classification - CCXR (5):
257/706

Current US Cross Reference Classification - CCXR (6):
257/718

US-PAT-NO: 6064573

DOCUMENT-IDENTIFIER: US 6064573 A

TITLE: Method and apparatus for efficient conduction cooling of surface-mounted integrated circuits

DATE-ISSUED: May 16, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Morton; James R.	Valencia	CA	N/A	N/A

US-CL-CURRENT: 361/704, 165/185 , 174/16.3 , 257/713 , 257/E23.09 , 361/710 , 361/715 , 361/717

ABSTRACT:

A plurality of heat-conducting compressible button contacts (10) between a heatsink (28) and an electronic part, e.g., a printed wiring board (22) or integrated circuit (24), to be cooled. A thin plate (16) and/or indentations (44, 44') in the heatsink are preferably used to support the heat-conducting buttons. Each heat-conducting button contact is placed in compression, generally, for example, by the heatsink. A thermal path is thus provided between the part and the heatsink. Differently sized compressible button contacts are used to accommodate disparate heights between the heat sink and surfaces on components of the electronic part.

12 Claims, 6 Drawing figures

Exemplary Claim Number: 4

Number of Drawing Sheets: 2

---------- KWIC ---------

Detailed Description Text - DETX (2):

As depicted in FIG. 1, a thermally conductive compressible button contact 10 comprises one or more randomly wound wires or filaments 12 formed into a specific height and diameter, ranging from 0.020" in diameter by 0.032" in height and upwards. As such, it has the appearance of a beam-like pillar. Such a button is produced by Cinch, a Division of Labinal Components & Systems, Inc., and described in their brochure entitled "CIN::APSE.TM. High Density Interconnect Technology" bearing an identification "10M894 CA-10" which describes its **button contact** as "constructed of randomly wound molybdenum **wire** which is formed into a specific height and diameter. Standard CIN::APSE contact diameters are 0.020" and 0.040"." It is used as an electrical contact in various electrical applications. A copy of the brochure is enclosed as part of the application file. Its use in the present invention is as a conductor of thermal, rather than of electrical, energy.

Current US Cross Reference Classification - CCXR (3):

257/713

Current US Cross Reference Classification - CCXR (4):

257/E23.09

US-PAT-NO: 5953214

DOCUMENT-IDENTIFIER: US 5953214 A

TITLE: Dual substrate package assembly coupled to a conducting member

DATE-ISSUED: September 14, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Dranchak; David William	Endwell	NY	N/A	N/A
Kelleher; Robert Joseph	Endicott	NY	N/A	N/A
Pagnani; David Peter	Endicott	NY	N/A	N/A
Zippetelli; Patrick Robert	Endwell	NY	N/A	N/A

US-CL-CURRENT: 361/767, 257/686 , 257/697 , 324/755 , 361/784 , 361/785 , 361/790 , 361/791 , 361/803 , 439/591

ABSTRACT:

An electronic package assembly for being electrically connected to a conducting member (e.g., a printed circuit board) wherein the assembly includes a pair of substrates. The first substrate includes opposing circuit patterns, those on one surface being of higher density and thus adapted for having high density electronic devices mounted thereon. This high density pattern is electrically coupled to the lesser density second pattern which is connected to contacts of a second substrate. These contacts are of the lesser density also, and extend through a dielectric member for being coupled to conductors (e.g., copper circuit pads) on the conducting member. Ready separability of various parts of the assembly is thus assured.

18 Claims, 3 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 3

---------- KWIC ---------

Detailed Description Text - DETX (34):

Electronic package assembly 50 further includes a second dielectric substrate 60 and an array of second conductors 61 therein. In this embodiment, second substrate 60 and second conductor(s) 61 are implemented as an area array interposer-style connector. Such a connector may be implemented in many different ways. In one example, a dielectric elastomer may be used which includes therein a plurality of conductive paths, e.g., small diameter wires, small conductive traces, or a more or less columnar series of conductive (or conductively plated) material, to provide the necessary interconnections. In another example, a very fine (typically 0.001- to 0.002-inch diameter) gold-plated wire, typically of a material such as beryllium-copper, copper-silver, or molybdenum, is formed and compressed into a "button-like" contact that is inserted into one of a series of uniformly-spaced openings in the dielectric substrate.

Current US Cross Reference Classification - CCXR (1):
257/686

Current US Cross Reference Classification - CCXR (2):
257/697

US-PAT-NO: 5701233

DOCUMENT-IDENTIFIER: US 5701233 A

TITLE: Stackable modules and multimodular assemblies

DATE-ISSUED: December 23, 1997

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Carson; John C.	Corona del Mar	CA	N/A	N/A
DeCaro; Robert E.	San Juan Capistrano	CA	N/A	N/A
Hsu; Ying	Huntington Beach	CA	N/A	N/A
Miyake; Michael K.	Westminster	CA	N/A	N/A

US-CL-CURRENT: 361/735, 257/685 , 257/686 , 257/723 , 257/777 , 257/E25.011 , 361/733 , 361/744 , 361/761 , 361/764 , 361/790 , 361/803 , 439/66 , 439/91

ABSTRACT:

Stacked, multimodular circuit assemblies are provided which comprise stacked, resealable, modules containing electronic circuitry, each module having a plurality of electrically conductive, embedded through-vias between the upper and major surfaces thereof. The through-vias are contained within the module matrix outside of the circuit-containing cavity or "tub" of the module and within the outer edges of the module body. Electronic circuitry contained in the module cavity is electrically connected to the through-vias by signal traces or vias passing out of the cavity and into contact with the through-vias, and adjacent modules are electrically interconnected by a resealable, multichannel connector array between adjacent modules having electrically conductive channels coupling opposing through-vias of the adjacent modules. The connector arrays can also serve to seal the assembly when the entire assemblage of modules is compressed and to connect the stacked modular assembly to exterior circuitry such as a printed circuit board or other device. Methods are also provided for assembling and electrically interconnecting electronic components within such stacked multimodular assemblies by attaching components of an electronic circuit to at least two stackable modules of the type described within the cavity thereof, interconnecting the circuit components with the described through-vias, and stacking and interconnecting the stackable modules with the described multichannel connector arrays interposed between each adjacent module pair.

24 Claims, 19 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

---------- KWIC ---------

Detailed Description Text - DETX (24):

FIGS. 13(A), (B), and (C) illustrate variations of the button contacts illustrated in FIG. 12 which are also available from Cinch Connectors, Inc., with FIG. 13(A) showing an expanded view of the button contact 91 of FIG. 12 in dielectric substrate 90. FIG. 13(B) illustrates a similar contact comprising

non-conductive cylinder 100 containing conductive pin 101 on either end of which are mounted compressible randomly wound conductive wire contacts 102, such as the button contacts 91 of FIGS. 12 and 13(A). FIG. 13(C) illustrates yet another variation of these contacts showing a dielectric substrate 105 containing conductive metal pin 106 opposed by compressible, randomly wound conductive wire button or cylinder 107.

Current US Cross Reference Classification - CCXR (1):
257/685

Current US Cross Reference Classification - CCXR (2):
257/686

Current US Cross Reference Classification - CCXR (3):
257/723

Current US Cross Reference Classification - CCXR (4):
257/777

Current US Cross Reference Classification - CCXR (5):
257/E25.011

US-PAT-NO: 5485351

DOCUMENT-IDENTIFIER: US 5485351 A

TITLE: Socket assembly for integrated circuit chip package

DATE-ISSUED: January 16, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hopfer; Albert N.	Park Ridge	IL	N/A	N/A
Allard; Edward M.	Des Plaines	IL	N/A	N/A

US-CL-CURRENT: 361/704, 257/E23.086 , 361/785 , 439/331 , 439/487 , 439/73

ABSTRACT:

A socket assembly for mechanically and electrically coupling an integrated component with an interfacing carrier includes a socket body for receiving the integrated component, a retaining spring hingedly connected to the socket body for retaining the integrated component within the socket body, and at least one post element. The socket body includes at least one generally cylindrical receiving member having at least a portion protruding through an aperture in the interfacing carrier which is deformable to engage the socket body with the carrier when the post element is received within the receiving element. The socket body also includes a first mounting surface having plurality of holes for receiving wadded button contacts and a heat transfer element in contacting relation with the mounting side of the integrated component.

94 Claims, 9 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Detailed Description Text - DETX (20):

Use of conductive electrical contacts 38 for the purposes of effecting electrical connections is known in the art. Each wadded wire electrical contact 38 is formed to fit within its receiving opening in circuit board 18 as illustrated in FIG. 6 so as to be frictionally gripped thereby in the central area for retention of the button contact in the board but so as to not restrict the ability of at least its end portions to function as a resilient spring member. As noted earlier, the electrical contact 25 can include additional elements, such as plungers, as shown in U.S. Pat. No. 5,127,837.

Current US Cross Reference Classification - CCXR (1):

257/E23.086

US-PAT-NO: 4581679

DOCUMENT-IDENTIFIER: US 4581679 A

TITLE: Multi-element circuit construction

DATE-ISSUED: April 8, 1986

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Smolley; Robert	Porteughese Bend	CA	N/A	N/A

US-CL-CURRENT: 361/742, 257/E23.172 , 361/729 , 361/785 , 361/792 , 439/66

ABSTRACT:

A packaging construction for electronic circuit package elements, such as printed circuit boards and integrated-circuit chip packages, to obviate the need for connector cables, back-panel wiring and similar techniques. Circuit packaging elements are interconnected through an interconnection medium that includes an insulated board with opening through it, and a number of connector elements in the form of compressible wads of conductive wire. The connector elements are disposed in selected openings in the insulated board and compressed into contact with contact areas formed on the circuit package elements. Shorter lead lengths and improved circuit operating speed are the principal results of the approach. In a three-dimensional construction employing the principles of the invention, chip packages are arranged in modules, and interconnections may be made between chip packages within each module, tranversely between modules, and in a third direction between layers of modules. The construction provides direct interconnections without the use of solder, connector cables or multilayer circuit boards, and makes most effective use of high-speed integrated circuitry.

6 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Detailed Description Text - DETX (4):

The buttons 20 as employed in these illustrative embodiments are fabricated using 0.002 inch beryllium copper wire, which is gold plated and wadded into a nearly cylindrical button of 0.042 inch diameter and length. The button under compression makes multiple contacts with a contact pad, and provides multiple conductive paths through the structure. In addition, each **contact** made by the **button** is at a very high pressure, because of the type of spring formed by the wadded **wire** and the small area of each **contact** point.

Current US Cross Reference Classification - CCXR (1):

257/E23.172

US-PAT-NO: 4574331

DOCUMENT-IDENTIFIER: US 4574331 A

TITLE: Multi-element circuit construction

DATE-ISSUED: March 4, 1986

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Smolley; Robert	Porteughese Bend	CA	N/A	N/A

US-CL-CURRENT: 361/735, **257/E23.172** , 361/736 , 361/790 , 439/74

ABSTRACT:

A packaging construction for electronic circuit package elements, such as printed circuit boards and integrated-circuit chip packages, to obviate the need for connector cables, back-panel wiring and similar techniques. Circuit packaging elements are interconnected through an interconnection medium that includes an insulated board with opening through it, and a number of connector elements in the form of compressible wads of conductive wire. The connector elements are disposed in selected openings in the insulated board and compressed into contact with contact areas formed on the circuit package elements. Shorter lead lengths and improved circuit operating speed are the principal results of the approach. In a three-dimensional construction employing the principles of the invention, chip packages are arranged in modules, and interconnections may be made between chip packages within each module, transversely between modules, and in a third direction between layers of modules. The construction provides direct interconnections without the use of solder, connector cables or multilayer circuit boards, and makes most effective use of high-speed integrated circuitry.

5 Claims, 6 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

---------- KWIC ---------

Detailed Description Text - DETX (4):

The buttons 20 as employed in these illustrative embodiments are fabricated using 0.002 inch beryllium copper wire, which is gold plated and wadded into a nearly cylindrical button of 0.042 inch diameter and length. The button under compression makes multiple contacts with a contact pad, and provides multiple conductive paths through the structure. In addition, each **contact** made by the **button** is at a very high pressure, because of the type of spring formed by the wadded **wire** and the small area of each **contact** point.

Current US Cross Reference Classification - CCXR (1):

257/E23.172

US-PAT-NO: 4355082

DOCUMENT-IDENTIFIER: US 4355082 A

TITLE: Ultra-thin wire for semiconductor connections

DATE-ISSUED: October 19, 1982

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Bischoff; Albrecht	Bruchkobel	N/A	N/A	DE
Aldinger; Fritz	Rodenbach	N/A	N/A	DE

US-CL-CURRENT: 428/607, 257/781 , 428/620 , 428/652 , 428/923

ABSTRACT:

To prevent metal fatique, particularly when making a button loop, or nail head thermo compression bond connection to a semiconductor, the connecting wire has a core of copper, or a copper alloy of at least 60% copper content, and a jacket of aluminum, or aluminum alloy, of at least 95% aluminum content; in a preferred form, the core is 94% copper and 6% tin, and the jacket is, for example, 99% aluminum, 1% silicon; 96% aluminum, 4% copper; or 99% aluminum, 1% magnesium, all percentages by weight.

10 Claims, 2 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 1

---------- KWIC ---------

Brief Summary Text - BSTX (7):

It is an object to provide an ultra-thin bonding or connecting **wire,** particularly for semiconductor bonding, which does not utilize noble metals but which has, nevertheless, high mechanical strength, is resistant to metal fatigue failure, and can be used in accordance with the **button** or nail head **contact** welding connecting process without danger of failure.

Current US Cross Reference Classification - CCXR (1):

257/781

US-PAT-NO: 4954875

DOCUMENT-IDENTIFIER: US 4954875 A

TITLE: Semiconductor wafer array with electrically conductive compliant material

DATE-ISSUED: September 4, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Clements; Ken	Santa Cruz	CA	N/A	N/A

US-CL-CURRENT: 257/686, 257/722 , 257/774 , 257/E21.597 , 257/E23.01 , 257/E23.011 , 257/E23.174 , 257/E25.013

ABSTRACT:

A semiconductor wafer array comprising a plurality of wafers of semiconductor material. Each of the wafers is provided with cone-shaped or pyramid-shaped vias. Inserted in each of the vias is a correspondingly shaped wad of electrically conductive compliant material for forming continuous vertical electrical connections between the wafers in the stack. The base of each wad makes connection to a bonding pad on the surface of a lower wafer as well as to the electrically conductive compliant material in the lower wafer.

21 Claims, 15 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 5

---------- KWIC ---------

Brief Summary Text - BSTX (13):

In applications requiring fewer vertical feedthroughs which thus lessen the need for very small vias and the use of an electrically conductive liquid to form the vertical electrical connections, it is found that vias which are somewhat larger may be filled with an electrically conductive compliant material. Such material may, for example, comprise wads of very fine **wire or wads** of electrically conductive elastomeric material.

Brief Summary Text - BSTX (19):

In view of the foregoing, principal objects of the present invention are a method and apparatus comprising a semiconductor wafer array in which the individual wafers in the array, as distinguished from printed circuit boards, are stacked one on top of another and vertically electrically interconnected using an electrically conductive compliant material such as a wad of fine **wire or a wad** of electrically conductive elastomer.

Detailed Description Text - DETX (12):

Referring to FIG. 11, there is provided in each of the vias 25 a wad of electrically conductive compliant material 45. In one of the embodiments of the present invention, the wad 45 comprises a wad of single strand fine wire. The shape of the wad 45 is roughly that of a pyramid or a cone. The diameter of the wire used to make the wad 45 is approximately 1/10th that of the width of the top side aperture 41, i.e. 1 mil, and the volume of the wire used is

such as to fill the vias 25 to within 10 to 20% of their volume; the remainder of the via volume comprising the air space between the wire in the wad. Any suitable conventional means may be used for pre-forming the wads 45 into the desired shape.

Detailed Description Text - DETX (15):

As an alternative to the fine wire wads 45 of FIG. 12, FIG. 13 shows a shaped form of conventional compliant conductive elastomer 51. A plurality of wads 51 may be used in place of wads 45 if desired.

L Number	Hits	Search Text	DB	Time stamp
1	5	wire adj wad$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:21
2	573	wire with button with contact	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:22
3	0	257/$.ccls. and 438/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:50
4	12	257/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:22
5	0	438/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:50

L Number	Hits	Search Text	DB	Time stamp
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4	1		USPAT	2004/01/02 12:15
5	1		USPAT	2004/01/02 12:16
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7	1		USPAT	2004/01/02 12:18
8	1		USPAT	2004/01/02 12:19
9	1		USPAT	2004/01/02 12:19
10	50547	crystal$1 same particle$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:10
11	78	lump$1 and blob$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:41
12	6	(lump$1 and blob$1) and (crystal$1 same particle$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:44
13	1761	microcrystalline near5 film$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:06
14	125	(crystal$1 same particle$1) and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:45
15	598	257/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:52
16	125	(crystal$1 same particle$1) and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:46
17	10	geometr$6 and ((crystal$1 same particle$1) and (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:10
18	3	361/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:54
19	130	428/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:58
20	22	(428/$.ccls. and (microcrystalline near5 film$1)) and (crystal$1 same particle$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:55

21	390	438/$.ccls. and (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:58
23	1	geometr$6 and ((crystal$1 same particle$1) and (438/$.ccls. and (microcrystalline near5 film$1)))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:58
22	27	(crystal$1 same particle$1) and (438/$.ccls. and (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:59
24	1	solderless same (crystal$1 same particle$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:08
25	1	solderless same (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:08
26	1	connector$1 same (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:09
27	317	crystal$1 same (microcrystalline near5 film$1)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:10
28	0	geometr$6 same (crystal$1 same (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:11
29	12	shape$1 same (crystal$1 same (microcrystalline near5 film$1))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 13:11
-	5	wire adj wad$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:40
-	573	wire with button with contact	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:22
-	0	257/$.ccls. and 438/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:50
-	12	257/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 12:45
-	0	438/$.ccls. and (wire with button with contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/01/02 09:50

US-PAT-NO: 5937282

DOCUMENT-IDENTIFIER: US 5937282 A

TITLE: Method for producing semiconductor device

DATE-ISSUED: August 10, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Nakajima; Setsuo	Kanagawa	N/A	N/A	JP
Yamazaki; Shunpei	Tokyo	N/A	N/A	JP
Kusumoto; Naoto	Kanagawa	N/A	N/A	JP
Teramoto; Satoshi	Kanagawa	N/A	N/A	JP

US-CL-CURRENT: 438/149, 257/E21.134 , 257/E21.413 , 257/E21.472 , 438/151 , 438/487

ABSTRACT:

In producing a thin film transistor, after an amorphous silicon film is formed on a substrate, a nickel silicide layer is formed by spin coating with a solution (nickel acetate solution) containing nickel as the metal element which accelerates (promotes) the crystallization of silicon and by heat treating. The nickel silicide layer is selectively patterned to form island-like nickel silicide layer. The amorphous silicon film is patterned. A laser light is irradiated while moving the laser, so that crystal growth occurs from the region in which the nickel silicide layer is formed and a region equivalent to a single crystal (a monodomain region) is obtained.

25 Claims, 22 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 9

---------- KWIC ---------

Brief Summary Text - BSTX (10):

On the other hand, there is a method for manufacturing a TFT using a crystalline silicon film which is far superior in characteristics as compared with the one using a thin film of amorphous silicon. The method for manufacturing TFT comprises the steps of: forming an amorphous silicon film; and modifying the resulting amorphous silicon film into a crystalline silicon film by subjecting the amorphous silicon film to heat treatment or to laser irradiation. The crystalline silicon film obtained by crystallizing an amorphous silicon film generally yields a polycrystalline structure or a microcrystalline structure.

Brief Summary Text - BSTX (16):

To overcome the problems concerning TFTs using a thin film of amorphous silicon or TFTs using a thin film of polycrystalline or microcrystalline silicon, a method for manufacturing a TFT using a particular region is known in the art. The method for manufacturing a TFT comprises steps of forming a region which can be regarded as a single crystal in a particular region of an

amorphous silicon thin film, and then forming a TFT utilizing this particular region. By employing the method, a TFT which exhibits characteristics well comparable to those of a transistor formed on a single crystal silicon wafer (i.e., a MOS type transistor) can be obtained.

Brief Summary Text - BSTX (53):

The quantity of the metal component to be introduced into the silicon semiconductor can be adjusted by controlling the concentration of the metal component in the solution. This method is particularly useful, because the concentration of the metal element to be finally introduced into the silicon film can be accurately controlled. In the method of introducing the metal element using the solution, a continuous layer can be formed on the surface of the semiconductor (or on the surface of the undercoating thereof) without forming island-like regions of metal **particles** for the crystallization. Then, a uniform and dense **crystal** growth can be effected by a crystallization method with heat treatment or with irradiation of laser light.

Current US Original Classification - CCOR (1):

438/149

Current US Cross Reference Classification - CCXR (4):

438/151

Current US Cross Reference Classification - CCXR (5):

438/487

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